WHAT IS CLAIMED IS:

1. For use in a receiver, a round off mechanism for maintaining a mean value of an operand comprising:

an incrementer selectively incrementing said operand at a most significant discard bit position to generate an incremented intermediate rounding result; and

control logic controlling an output of said round off mechanism, said control logic causing said round off mechanism to produce a rounded result equal to either

a remainder of said operand after truncation of bits within selected discard bit positions within said operand, said selected discard bit positions including said most significant discard bit position, or

a remainder of said incremented intermediate rounding result after truncation of bits within said selected discard bit positions within said incremented intermediate result.

2. The round off mechanism as set forth in Claim 1 wherein said control logic causes said round off mechanism to produce:

said remainder of said operand after truncation of said bits within said selected discard bit positions as said rounded result when said operand is

positive, or

negative and contains a logical one within said most significant discard bit position and at least one other bit position within said selected discard bit positions; and

said remainder of said incremented intermediate rounding result after said truncation of said bits within said selected discard bit positions as said rounded result when said operand is negative and contains

a logical zero within said most significant discard bit position, or

a logical one within said most significant discard bit position and logical zeros in any remaining discard bit positions.

3. The round off mechanism as set forth in Claim 1 wherein said control logic causes said round off mechanism to select between

said remainder of said operand after truncation of said bits within said selected discard bit positions, and

said remainder of said incremented intermediate rounding result after said truncation of said bits within said selected discard bit positions as said rounded result.

4. The round off mechanism as set forth in Claim 1 wherein said round off mechanism avoids any offset within said rounded result.

5. The round off mechanism as set forth in Claim 1 wherein said round off mechanism computes both said remainder of said operand after truncation of said bits within said selected discard bit positions and said remainder of said incremented intermediate rounding result after said truncation of said bits within said selected discard bit positions for said operand,

wherein said control logic causes said round off mechanism to select

said remainder of said operand after truncation of said bits within said selected discard bit positions as said rounded result when said operand is

positive, or

negative and contains a logical one within said most significant discard bit position and at least one other bit position within said selected discard bit positions, and

said remainder of said incremented intermediate rounding result after said truncation of said bits within said selected discard bit positions as said rounded result when said operand is negative and contains

a logical zero within said most significant discard bit position, or

a logical one within said most significant discard bit position and logical zeros in any remaining discard bit positions.

6. A receiver comprising:

a computation unit;

a round off mechanism receiving an operand from said computation unit and maintaining a mean value of said operand during rounding, said round off mechanism comprising:

an incrementer selectively incrementing said operand at a most significant discard bit position to generate an incremented intermediate rounding result; and

control logic controlling an output of said round off mechanism, said control logic causing said round off mechanism to produce a rounded result equal to either

a remainder of said operand after truncation of bits within selected discard bit positions within said operand, said selected discard bit positions including said most significant discard bit position, or

a remainder of said incremented intermediate rounding result after truncation of bits within said selected discard bit positions within said incremented intermediate result.

7. The receiver as set forth in Claim 6 wherein said control logic causes said round off mechanism to produce:

said remainder of said operand after truncation of said bits within said selected discard bit positions as said rounded result when said operand is

positive, or

negative and contains a logical one within said most significant discard bit position and at least one other bit position within said selected discard bit positions; and

said remainder of said incremented intermediate rounding result after said truncation of said bits within said selected discard bit positions as said rounded result when said operand is negative and contains

a logical zero within said most significant discard bit position, or

a logical one within said most significant discard bit position and logical zeros in any remaining discard bit positions.

8. The receiver as set forth in Claim 6 wherein said control logic causes said round off mechanism to select between

said remainder of said operand after truncation of said bits within said selected discard bit positions, and

said remainder of said incremented intermediate rounding result after said truncation of said bits within said selected discard bit positions

as said rounded result.

9. The receiver as set forth in Claim 6 wherein said round off mechanism avoids any offset within said rounded result.

10. The receiver as set forth in Claim 6 wherein said round off mechanism computes both said remainder of said operand after truncation of said bits within said selected discard bit positions and said remainder of said incremented intermediate rounding result after said truncation of said bits within said selected discard bit positions for said operand,

wherein said control logic causes said round off mechanism to select

said remainder of said operand after truncation of said bits within said selected discard bit positions as said rounded result when said operand is

positive, or

negative and contains a logical one within said most significant discard bit position and at least one other bit position within said selected discard bit positions, and

said remainder of said incremented intermediate rounding result after said truncation of said bits within said selected discard bit positions as said rounded result when said operand is negative and contains

a logical zero within said most significant discard bit position, or

a logical one within said most significant discard bit position and logical zeros in any remaining discard bit positions.

11. For use in a receiver, a method of maintaining a mean value of an operand during rounding comprising:

selectively incrementing the operand at a most significant discard bit position to generate an incremented intermediate rounding result; and

producing a rounded result equal to either

a remainder of the operand after truncation of bits within selected discard bit positions within the operand, the selected discard bit positions including the most significant discard bit position, or

a remainder of the incremented intermediate rounding result after truncation of bits within the selected discard bit positions within the incremented intermediate result.

12. The method as set forth in Claim 11 wherein the step of producing a rounded result further comprises:

producing the remainder of the operand after truncation of the bits within the selected discard bit positions as the rounded result when the operand is

positive, or

negative and contains a logical one within the most significant discard bit position and at least one other bit position within the selected discard bit positions; and

producing the remainder of the incremented intermediate rounding result after the truncation of the bits within the selected discard bit positions as the rounded result when the operand is negative and contains

a logical zero within the most significant discard bit position, or

a logical one within the most significant discard bit position and logical zeros in any remaining discard bit positions.

13. The method as set forth in Claim 11 wherein the step of producing a rounded result further comprises:

selecting between the remainder of the operand after truncation of the bits within the selected discard bit positions and the remainder of the incremented intermediate rounding result after the truncation of the bits within the selected discard bit positions.

14. The method as set forth in Claim 11 wherein the step of producing a rounded result avoids any offset within the rounded result.

15. The method as set forth in Claim 11 wherein the step of producing a rounded result further comprises:

computing both the remainder of the operand after truncation of the bits within the selected discard bit positions and the remainder of the incremented intermediate rounding result after the truncation of the bits within the selected discard bit positions for the operand;

selecting the remainder of the operand after truncation of the bits within the selected discard bit positions as the rounded result when the operand is

positive, or

negative and contains a logical one within the most significant discard bit position and at least one other bit position within the selected discard bit positions; and

selecting the remainder of the incremented intermediate rounding result after the truncation of the bits within the selected discard bit positions as the rounded result when the operand is negative and contains

a logical zero within the most significant discard bit position, or

a logical one within the most significant discard bit position and logical zeros in any remaining discard bit positions.

16. A computer program product within a computer usable medium for maintaining a mean value of an operand during rounding comprising:

instructions for selectively incrementing the operand at a most significant discard bit position to generate an incremented intermediate rounding result; and

instructions for producing a rounded result equal to either

a remainder of the operand after truncation of bits within selected discard bit positions within the operand, the selected discard bit positions including the most significant discard bit position, or

a remainder of the incremented intermediate rounding result after truncation of bits within the selected discard bit positions within the incremented intermediate result.

17. The computer program product as set forth in Claim 16 wherein the instructions for producing a rounded result further comprise:

instructions for producing the remainder of the operand after truncation of the bits within the selected discard bit positions as the rounded result when the operand is

positive, or

negative and contains a logical one within the most significant discard bit position and at least one other bit position within the selected discard bit positions; and

instructions for producing the remainder of the incremented intermediate rounding result after the truncation of the bits within the selected discard bit positions as the rounded result when the operand is negative and contains

a logical zero within the most significant discard bit position, or

a logical one within the most significant discard bit position and logical zeros in any remaining discard bit positions.

18. The computer program product as set forth in Claim 16 wherein the instructions for producing a rounded result further comprise:

instructions for selecting between the remainder of the operand after truncation of the bits within the selected discard bit positions and the remainder of the incremented intermediate rounding result after the truncation of the bits within the selected discard bit positions.

19. The computer program product as set forth in Claim 16 wherein the instructions for producing a rounded result avoid any offset within the rounded result.

20. The computer program product as set forth in Claim 16 wherein the instructions for producing a rounded result further comprise:

instructions for computing both the remainder of the operand after truncation of the bits within the selected discard bit positions and the remainder of the incremented intermediate rounding result after the truncation of the bits within the selected discard bit positions for the operand;

instructions for selecting the remainder of the operand after truncation of the bits within the selected discard bit positions as the rounded result when the operand is

positive, or

negative and contains a logical one within the most significant discard bit position and at least one other bit position within the selected discard bit positions; and

instructions for selecting the remainder of the incremented intermediate rounding result after the truncation of the bits within the selected discard bit positions as the rounded result when the operand is negative and contains

a logical zero within the most significant discard bit position, or

a logical one within the most significant discard bit position and logical zeros in any remaining discard bit positions.